UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,875	09/05/2000	Isao Nojiri	50006-073	7618

7590 02/22/2002

McDermott Will & Emery
600 13th Street N W
Washington, DC 20005-3096

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/654,875	Nojiri
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jan 4, 2002

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-9 is/are pending in the applica

4a) Of the above, claim(s) 7-9 is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-6 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 recites the limitation "said electrode" in line 6. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, lines 2-4 cite "said connection pad on said first semiconductor chip is connected with said connection pad on said second semiconductor chip through a bonding wire".

However, the description in the specification and Fig. 8-10 show the connection pad (52Y1) on the second semiconductor chip is connected with said connection pad on the first semiconductor chip through an electrode/solder (66 in Fig. 8-10) and wire/trace portion (58/60 in Fig. 8-10) and not through a bonding wire. Furthermore, page 21, line 13 cites "This allows the connection pads to be connected with another connecting portions without using wire bonding...".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Fukui et al (US Pat. 6100594) and Williams et al (US Pat. 5665996).

Regarding claims 1-3, the APA discloses a semiconductor device mounted on a mother board comprising:

- a circuit board (102 in Fig. 11/12) to be positioned on the mother board

- semiconductor chips (110, 112, etc. in Fig. 11/12) positioned on the circuit board, wherein

a) the circuit board has connection pads (104-1, 104-2, etc. in Fig. 11/12) spaced away from each other

b) the semiconductor chips have connection pads corresponding to the connection pads formed on the surface of the circuit board, and

c) the connection pads on the chips and the circuit board are electrically connected through bonding wires (116 in Fig. 11/12)

(Specification pp. 1-4; Fig. 11 and 12).

The APA fails to specify using a relay pad spaced away from the connection pad on the circuit board and having a wire portion or using a bonding wire to connect the two pads.

Fukui et al teach using pads on the circuit board comprising an elongated pad (13 showing two bonding wires in Fig. 7a) which has an inner/connection pad and an outer/relay pad (not numerically referenced in Fig. 7a) and they are connected with a wire portion/trace (Col. 10, line 30-42). Furthermore, Fukui et al teach forming the wiring portion/trace pattern using conventional deposition and photolithography/printing processes (Col. 7, line 30-60).

Williams et al teach using a conventional bonding wire (Fig. 6A/B) to connect the desired wiring portions (Col. 2, line 58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a relay pad spaced away from the connection pad on the circuit board and having a wire portion or using a bonding wire to connect the two pads to reduce the wire bonding defects and wire-shorting problem using Fukui et al and Williams et al's wiring design in the APA.

6. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Bertin et al (US Pat. 6294406) and Fukui et al (US Pat. 6100594).

Regarding claims 4-6, the APA discloses a semiconductor device mounted on a mother board comprising:

- a first semicontor chip (110 in Fig. 11/12) having connection pads (114-2 in Fig. 11/12)
- a second semiconductor chip positioned on the first chip and having connection pads (114-1, 114-3, etc. in Fig. 11/12)

(Specification pp. 1-4; Fig. 11 and 12).

The APA fails to specify having an electrode on the second chip such that the connection pads of the first and second chips are in a region facing each other and are electrically connected through an electrode/conductive member positioned in the region.

Bertin et al teach connecting the second chip positioned on the first chip using conventional flip chip bonding (40/30 in Fig. 5) such that the connection metal/solder pads of the first and second chips are in a region facing each other and are electrically connected through a conductive member/solder ball 50 in Fig. 5) positioned in the region (Col. 3, line 1-66).

Fukui et al teach using conventional methods such as face-up/wire bonding or face-down /flip chip bonding of the chips for connection of the chip pads/electrodes with a wiring pattern on the substrate (Fig. 13a and b; Col. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second chip being connected face-down to the first chip such that the connection pads of the first and second chips are in a region facing each other and are electrically connected through an electrode/conductive member positioned in the region to

improve interconnection density and to reduce the package dimensions using Bertin et al and Fukui et al's flip chip design in the APA.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Nitin Parekh

01-26-01